REMARKS

Claims 1, 32, and 38 have been amended. Claims 22 – 23, 34, 51, 53, and 57 have been canceled No new claims have been added. Claim 1-21, 24-33, and 35-50, 52, 54-56, and 58 are pending.

Applicant's representative is grateful for the indication of allowable subject matter in claims 15, 39, and 43. Applicant's representative is grateful for the allowance of claims 6-13, 24-31, 35-37, 45-48, 52, 54, and 58. (Claims 6-13 is listed in the list of allowed claims in the "Office Action Summary" but claims 6-13 is not included in the list of allowed claims on page 4 of the Office Action. However, claims 6-13 is assumed to be allowed as no rejection is directed to these claims.)

For clarity, in claims 1, 28-29, 30, 32, 35, 37, and 44, the expression (M/2 – 1) has been amended to instead read ((M/2) – 1).

Claims 18-23 and 32-34 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Mihara (U.S. Patent No. 5,418,923). Claims 1-5, 14, 38, 40-42, and 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mihara in view of Foss (U.S. Patent No. 6,580,652). Claims 49-51, 53, and 55-57 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mihara in view of Foss and Nataraj (U.S. Patent No. 6,757,779). These rejection are respectfully traversed.

Claim 1 recites, *inter alia,* "for k=0 to ((M/2) — 1), the respective binary codes provided by the output signals for the (2k)th and (2k+1)th input lines being complementary."

Claims 14, 49, and 55 recite, *inter alia,* "switching elements, each switching element controlling one of the output lines in response to an asserted input signal on one of the input lines; the switching elements that respond to an asserted input signal

on one of the input lines together providing a respective output signal on the output lines that is converted from the asserted input signal; each switching element having at most one neighboring switching element controlling the same output line."

Claim 18 recites, *inter alia,* "respective set of code bits on the output lines; the respective codes bits of each input line being complementary with the respective set of code bits of one of the input line's neighboring input lines."

Claim 32 recites, *inter alia,* "converting each input signal to a respective N-bit code; the respective N-bit code for each input signal being unique and between zero and (M—1); for k=0 to ((M/2)—1), the respective N-bit codes for the input signals with their (2k)th and (2k+1)th bits asserted being complementary."

Claim 38 recites, *inter alia,* "priority encoder circuitry that, ... provides an M-bit priority signal with at most one asserted bit, ... and address converter circuitry that, in response to each M-bit priority signal, provides a respective N-bit address code, where N is less than M and at least as great as $\log_2 M$; the respective N-bit address codes together being a non-ordinal encoding of the M-bit priority signals and a recoder circuitry that, in response to the respective N-bit address code of each M-bit priority signal, provides a recoded N-bit address code; the recoded N-bit address codes of the M-bit priority signals together being an ordinal encoding of the M-bit priority signals."

Claim 50 recites, *inter alia,* "converting circuitry that responds to the input signals and provides the codes on the output lines; for each input line, the converting circuitry providing a respective code in response to an asserted bit on the input line; each input line's respective code being complementary with the respective code of one of the input line's neighboring input lines."

Claim 56 recites, *inter alia*, "converting circuitry that responds to the input signals and provides the codes on the output lines; for each input line, the converting circuitry providing a respective code in response to an asserted bit on the input line; each input line's respective code being complementary with the respective code of one of the input line's neighboring input lines."

The identified claims and associated limitations are not shown or suggested in the cited references.

Mihara is directed a circuit for prioritizing outputs of an associative memory. Referring to Fig. 1, the Mihara discloses a priority determining circuit 1 which is coupled to a signal selection circuit 8 and an encoder 9. The priority determining circuit 7 is divided into a first sub-circuit 71 and a second sub-circuit 72. The two sub-circuits 71, 72 are triangular and arranged in a complementary fashion to minimize space requirements. The first sub-circuit 71 is associated with the high order match lines M5-M8. The second sub-circuit 72 is associated with the low order match lines M1-M7. The relative ordering of the high and low order match lines are reversed with respect to each other. The two sub-circuits 71, 72 of the priority determining circuit 7 cooperate to determine a highest priority match line and produce output to the signal selection circuit 8, which is encoded by the encoder 9.

As to claims 1, 18, 32, 50, and 56, contrary to the assertion in the Office Action, Mihara fails to disclose or suggest an encoder which produces complementary output codes for a (2k)th and (2k+1)th input line, where k ranges from 0 to ((M/2) – 1), or for neighboring input lines. For example, in encoder 9, if only match line M6 were asserted, then only arbitration signal T3 would be asserted, and the corresponding encoder output would be {0, 1, 0}. Similarly, if only match line M7 were asserted, then only arbitration signal T5 would be asserted, and the corresponding encoder output

would be {0, 0, 1}, which is not complementary to {0, 1, 0}. Mihara therefore fails to disclose or suggest:

> "for k=0 to ((M/2) − 1), the respective binary codes provided by the output signals for the (2k)th and (2k+1)th input lines being complementary"
> (as recited in claim 1);
>
> "respective set of code bits on the output lines; the respective codes bits of each input line being complementary with the respective set of code bits of one of the input line's neighboring input lines"
> (as recited in claim 18);
>
> "converting each input signal to a respective N-bit code; the respective N-bit code for each input signal being unique and between zero and (M−1); for k=0 to ((M/2)−1), the respective N-bit codes for the input signals with their (2k)th and (2k+1)th bits asserted being complementary"
> (as recited in claim 32);
>
> "converting circuitry that responds to the input signals and provides the codes on the output lines; for each input line, the converting circuitry providing a respective code in response to an asserted bit on the input line; each input line's respective code being complementary with the respective code of one of the input line's neighboring input lines"
> (as recited in claim 50); or
>
> "converting circuitry that responds to the input signals and provides the codes on the output lines; for each input line, the converting circuitry providing a respective code in response to an asserted bit on the input line; each input line's respective code being complementary with the respective code of one of the input line's neighboring input lines"
> (as recited in claim 56).

As to claims 14, 49, and 55, contrary to the Office Action , Mihara fails to disclose or suggest "switching elements, each switching element controlling one of the output lines in response to an asserted input signal on one of the input lines; the switching elements that respond to an asserted input signal on one of the input lines together providing a respective output signal on the output lines that is converted from

the asserted input signal; each switching element having at most one neighboring switching element controlling the same output line." The Office Action asserts that these switching elements are represented by "dotted connections" representing switching transistors. The undersigned has been unable to identify any dotted connection corresponding to the claimed switching elements. The only illustrated switching elements correspond to the transistors in the priority determining circuits 7, which does not correspond to the encoder 9 and further does not satisfy the condition of "at most one neighboring switching element controlling the same output line."

Mihara also fails to disclose or suggest a "recoder circuitry that, in response to the respective N-bit address code of each M-bit priority signal, provides a recoded N-bit address code; the recoded N-bit address codes of the M-bit priority signals together being an ordinal encoding of the M-bit priority signals.", as recited in claim 38.

The Office Action additionally cites to Foss (which discloses a priority encoder) and Nataraj (which discloses a content addressable memory). However, neither Folss nor Nataraj discloses or suggests the above recited features of the independent claims.

Accordingly, claims 1, 14, 18, 32, 49-50, and 55-56 are believed to be allowable over the prior art of record. Depending claims 2-5, 15-17, 19-21, 33, and 39-44 are also believed to be allowable for at least the same reasons as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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